REMARKS

Claims 1-11 and 18-20 are presented for examination, of which claims 1 and 18 are in independent form.

Claims 1-4, 6, 7, 18 and 19 have been amended by the present response. In addition, non-elected claims 12-17 are cancelled without prejudice, limitation or waiver. Support for the amendments may be found in the present patent application in respect of Figure 5 and associated description at Paragraphs [0041] and [0042], *inter alia*.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding Election/Restriction

Responsive to the requirement set forth in Paragraph 5 of the pending Office Action, Applicant hereby affirms the election made without traverse of the invention defined by claims 1-11 and 18-20 in Group I.

Regarding Amendments to the Specification

The Examiner has objected to the disclosure in the currently outstanding Office Action. In response, Paragraphs **[0002]**, **[0024]**, **[0026]** and **[0046]** of the original specification have been amended to include updated information regarding the cross-referenced related applications and to remove informalities noted by the Examiner. Paragraph **[0003]** was also cited, but Applicant could identify no blank lines in this paragraph. The objections to the specification are now believed to be overcome or otherwise rendered moot.

Regarding the Claim Rejections - 35 U.S.C. §112

In the pending Office Action, claim 1 is rejected under 35 U.S.C. §112, second paragraph, for insufficient antecedent basis. This claim has been amended consistent with the comments provided by the Examiner. It is therefore believed that the pending §112 rejection has been overcome or otherwise rendered moot.

Regarding the Claim Rejections - 35 U.S.C. §102(e)

Claims 1, 4, 5, 10, 11 and 18-20 are rejected in the pending Office Action under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,826,247 in the name of Elliot et al. (hereinafter the *Elliott* reference). In connection with these rejections, the Examiner commented as follows with respect to base claim 1:

> **Elliott** teaches an increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising: a delay circuit block **(Fig. 5, delay chain 502, the phase detectors 505)** operable to receive and align at least a block of said debug data. Elliott also teaches a first mask circuit connected to said delay circuit block, wherein said first mask circuit is operable to select a first portion of said block of aligned debug data for incrementing and a second mask circuit connected to said delay circuit block, wherein said second mask circuit is operable to select a second portion of said block of aligned debug data for decrementing **(Fig. 5, the claimed first and second mask circuits are embodied in a Delay Measurement and Ambiguity Resolver (DM&AR) 512 that receives results from the delay chain phase detectors 505 and generates an increment or decrement signal to the Averaging Counter 514). Elliott** further teaches an accumulation circuit **(Fig. 5, Averaging Counter 514)** connected to said first mask circuit and said second mask circuit, said accumulation circuit for generating an accumulated value based on outputs provided by said first and second mask circuits. (Col. 8, l. 36 to col. 10, l. 28).

Applicant respectfully submits that the pending §102(e) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment.

As defined by base claim 1, an embodiment of the present disclosure is directed to an increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising, *inter alia*, a first mask circuit operable to select a first portion of a multi-bit block of debug data that is aligned, a second mask circuit operable to select a second portion of the aligned, multi-bit block of debug data and an accumulation circuit connected to the first mask circuit and the second mask circuit for generating an accumulated value using the first portion and the second portion.

Similarly, base claim 18 is directed to a computer system having an increment/decrement circuit for use with a general purpose performance counter connected to a bus carrying debug data, the increment/decrement circuit comprising, *inter alia*, means for receiving and aligning a multi-bit block of the debug data, means for selecting a first portion of the block of aligned

debug data, means for selecting a second portion of the block of aligned debug data and means for generating an accumulated value using the first portion and the second portion.

The *Elliott* reference appears directed to a digital phase lock loop and a high precision digital phase comparator circuit for use in digital electronic circuits. See column 3, lines 20-23. FIG. 5 of the *Elliott* reference is cited as showing the claimed increment/decrement circuit and is reproduced herein for convenience. In this figure, reference clock signal 504 can be delayed using delay chain 502, which is composed of discretely programmable delay elements 507. Configuring all of the elements in delay chain 502 controls the total delay through delay chain 502. When this is combined

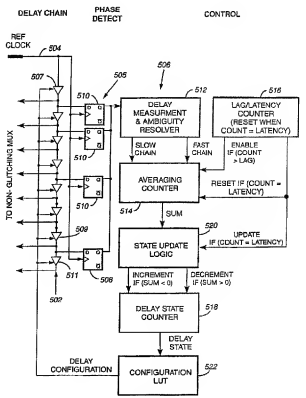

FIG. 5

with the results of phase detectors 505, the digital delay locked loop (DLL) system of FIG. 5 is able to lock in phase with the reference clock. See column 8, lines 36-64. The delay chain is controlled by control subsystem 506, which contains delay measurement and ambiguity resolver 512 and averaging counter 514. Base claim 1, as currently constituted, is distinguishable over *Elliott* in a number of ways. The claimed circuit receives and operates on a multi-bit block of debug data, while the circuit of *Elliott* receives and acts on a clock signal. Further, the claimed first and second mask circuits are operable to select first and second portions of the multi-bit block of debug data, with the first and second portions being used to generate the accumulation value. In contrast, the delay measurement and ambiguity resolver circuit 512 of *Elliott* receives results from phase detectors 505 and based on the information from the phase detection, generates an increment or decrement signal to averaging counter 514 based on whether the measured delay of delay chain 502 is too fast or too slow. *Elliott* does not select first and second portions of the "data" signal. See column 9,

lines 38-45. Base claim 18 is also distinguishable over the *Elliott* reference for similar reasons.

Based on the foregoing, Applicant respectfully submits that base claims 1 and 18 are not anticipated or suggested by the applied art of record, and are therefore in condition for allowance. Claims 4, 5, 10 and 11 depend from base claim 1 and introduce additional limitations therein. Likewise, claims 19 and 20 depend from base claim 18 and introduce additional limitations therein. Accordingly, these dependent claims are also believed to be in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Claims 2, 3 and 6-9 are rejected in the pending Office Action under 35 U.S.C. §103(a) as being unpatentable over *Elliott*, either alone or in combination with one of U.S. Patent No. 5,913,229 in the name of Joo (hereinafter the *Joo* reference) or U.S. Patent No. 6,275,782 in the name of Mann (hereinafter the *Mann* reference) or U.S. Patent Application Publication No. 2001/0005408 in the name of Neukom (hereinafter the *Neukom* reference.

Claims 2, 3 and 6-9 depend from base claim 1 and are distinguishable over the applied art for the same reasons as set forth above with respect to claim 1 inasmuch as *Elliot* continues to be relied upon as the primary reference for §103 purposes. As discussed previously, *Elliott* does not act on a multi-bit block of debug data, but on a clock signal. Additionally, the delay measurement and ambiguity resolver circuit 512 of *Elliott* generates an increment signal or a decrement signal to averaging counter 514 based on whether the measured delay of delay chain 502 is too fast or too slow, but does not disclose selecting first and second portions of a multi-bit block of debug data and using the first and second portions to generate an accumulated value. The additional references, i.e., *Joo*, *Mann* and *Neukom*, do not cure, either alone or in any reasonable combination, the above deficiencies of *Elliott*.

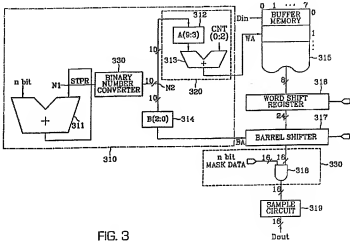

FIG. 3

The *Joo* reference is directed to a buffer memory controller that stores sampled data having variable bit length. See Abstract. In FIG. 3, reproduced hereinabove for convenience, masking circuit 330 of *Joo* discloses a multi-bit mask that is ANDed with a multi-bit signal. However, Applicant submits that even if *Joo* were combined with *Elliott*, as suggested in the rejection, the use of a multi-bit mask would provide no benefit to the circuit of *Elliott*. *Elliott* receives a clock signal, not a multi-bit data signal, so there is no clear manner in which these references might be combined to yield an operable result. Accordingly, there is no motivation to combine the references in the suggested manner. Additionally, *Joo* does not disclose selecting first and second portions of a multi-bit block of debug data and using the first and second portions to generate an accumulated value.

The *Mann* reference is directed to performance monitoring in integrated circuits using an adaptive adder circuit. See Abstract. In the adaptive adder circuit, shown in FIG. 2 and reproduced hereinbelow for convenience, the input data stream of *Mann* is a serially-provided sample of a performance parameter

being measured, such as cache hit information. The performance parameter value is XOR'd with a compare signal 204 output by comparator 203. If the performance parameter value and the compare signal 204 are equal, clock signal 209 is blocked and no value is added to or subtracted from counter 201. If the two values differ, clock signal 209 will pass to counter 201 as signal 210. Counter 201 will be added to or subtracted from depending on the value of the compare signal 204. See column 3, line 20 through column 4, line 12. However, *Mann* does not disclose selecting first and second portions of a multi-bit block of debug data and using the first and second portions to generate an accumulated value as currently claimed.

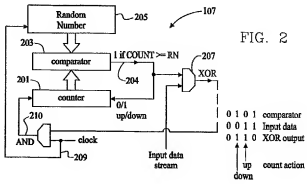

FIG. 2

The *Neukom* reference is directed to a device with a frequency synthesizer in which jitter is reduced without an accurate linear phase detector or high precision phase to voltage conversion. See paragraph [0006]. FIG. 3 of *Neukom*, reproduced

herein for convenience, discloses an accumulator adder circuit. In this figure, *Neukom* discloses increment register 30 and decrement register 31 wherein the content of one of increment register 30 and decrement register 31 is selected at multiplexer 32 and added to adder circuit 34. Accumulator 36 receives a clock input and outputs a frequency divided output signal. *Neukom*, like *Elliott*, does not act on a multi-bit block of debug data, but on a clock signal. See Paragraphs [0015] and [0033]-[0034]. Accordingly, *Neukom* does not disclose the claimed features relating to selecting first and second portions of a multi-bit block of debug data and using the first and second portions to generate an accumulated value.

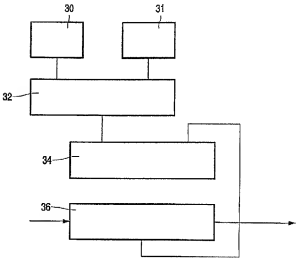

FIG. 3

Accordingly, at a minimum, the applied references, either alone or in any reasonable combination, fail to teach or suggest all the limitations of the claims. Dependent claims 2, 3 and 6-9

are therefore believed to be in condition for allowance over the art of record.

SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: August 22, 2008

/Shreen K. Danamraj/
Shreen K. Danamraj
Registration No. 41,696

Correspondence Address

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Please direct telephone calls to:

Steven L. Webb
(970) 898-3451